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L2: Entry 1 of 4 File: USPT Feb 10, 2004

DOCUMENT-IDENTIFIER: US 6691270 B2
TITLE: Integrated circuit and method of operation of such a circuit employing serial test scan chains

Abstract Text (1):
The present invention provides a technique for operating an integrated circuit comprising a plurality of circuit elements, with a plurality of serial test scan chains, each being coupled to a different one of the circuit elements. A scan chain selector is responsive to a specified scan chain specifying value to select a corresponding one of the plurality of test scan chains. A scan chain controller is also provided which has a serial interface for receiving signals from outside of the integrated circuit, the scan chain controller comprising an instruction decoder for decoding scan chain controller instructions received from the serial interface. In accordance with the present invention, the decoder is responsive to a first scan chain controller instruction to specify a pre-determined scan chain specifying value and a second scan chain controller instruction for decoding by the decoder. The provision of such a first scan chain controller instruction enables the efficiency of the testing procedure to be improved.

Brief Summary Text (12):
Viewed from a first aspect, the present invention provides an integrated circuit comprising: a plurality of circuit elements; a plurality of serial test scan chains each coupled to a different one of said circuit elements; a scan chain selector responsive to a specified scan chain specifying value to select a corresponding one of said plurality of test scan chains; a scan chain controller having a serial interface for receiving signals from outside of said integrated circuit, said scan chain controller comprising an instruction decoder for decoding scan chain controller instructions received from said serial interface; the decoder being responsive to a first scan chain controller instruction to specify a predetermined scan chain specifying value and a second scan chain controller instruction for decoding by the decoder.

Brief Summary Text (14):
In preferred embodiments, the integrated circuit further comprises: an instruction register for storing a scan chain controller instruction to be decoded by the decoder; and a scan chain register for storing a scan chain specifying value to be referenced by the scan chain selector to determine which test scan chain to select. Typically, both the instruction register and the scan chain register will reside within the scan chain controller, as will the scan chain selector in preferred embodiments.

Brief Summary Text (18):
Further, in preferred embodiments, the integrated circuit further comprises a second multiplexer located between the scan chain register and the scan chain selector having a first input connected to the scan chain register and a second input arranged to receive the predetermined scan chain specifying value, the pre-decoder being responsive to the first scan chain controller instruction to cause the second multiplexer to output the data received at the second input.

Brief Summary Text (20):

In such preferred embodiments, the decoder is preferably responsive to the second scan chain controller instruction to cause the scan chain selector to be coupled to the serial interface to enable instruction data received at the serial interface to be passed to the shift register of the test scan chain identified by the predetermined scan chain specifying value. Hence, decoding of the first scan chain controller instruction will cause the test scan chain associated with the instruction transfer register to be selected, and the scan chain selector to be coupled to the serial interface to enable instruction data to subsequently be passed in through the serial interface to the shift register of the test scan chain.

Brief Summary Text (21):
Further, in preferred embodiments, once the instruction data has been shifted into the shift register, it is written into the instruction transfer register, and the microprocessor is caused to execute the instruction specified by the instruction data, with the resulting data being written to a data transfer register. In preferred embodiments, the second scan chain controller instruction that is specified via the first scan chain controller instruction actually causes the coupling of the scan chain selector to the serial interface, and the subsequent writing of the instruction data into the instruction transfer register from the shift register. Preferably, the scan chain controller then returns to a mode of operation which, in combination with the second scan chain controller instruction still being set, causes a signal to be issued to the microprocessor to cause it to execute the instruction specified by the instruction data in the instruction transfer register.

Brief Summary Text (23):
In preferred embodiments, once data has been written to the data transfer register, a third scan chain controller instruction is input to the scan chain controller, the decoder being responsive to the third scan chain controller instruction to cause the scan chain selector to be coupled to the serial interface to enable the data in the data transfer register to be stored into the shift register of the test scan chain coupled to the data transfer register and then output over the serial interface.

CLAIMS:

1. An integrated circuit comprising: a plurality of circuit elements; a plurality of serial test scan chains each coupled to a different one of said circuit elements; a scan chain selector responsive to a specified scan chain specifying value to select a corresponding one of said plurality of test scan chains; a scan chain controller having a serial interface for receiving signals from outside of said integrated circuit, said scan chain controller comprising an instruction decoder for decoding scan chain controller instructions received from said serial interface; the decoder being responsive to a first scan chain controller instruction to specify a predetermined scan chain specifying value and a second scan chain controller instruction for decoding by the decoder.

2. An integrated circuit as claimed in claim 1, further comprising: an instruction register for storing a scan chain controller instruction to be decoded by the decoder; and a scan chain register for storing a scan chain specifying value to be referenced by the scan chain selector to determine which test scan chain to select.

5. An integrated circuit comprising: a plurality of circuit elements; a plurality of serial test scan chains each coupled to a different one of said circuit elements; a scan chain selector responsive to a specified scan chain specifying value to select a corresponding one of said plurality of test scan chains; a scan chain controller having a serial interface for receiving signals from outside of said integrated circuit, said scan chain controller comprising an instruction

decoder for decoding scan chain controller instructions received from said serial interface; the decoder being responsive to a first scan chain controller instruction to specify a predetermined scan chain specifying value and a second scan chain controller instruction for decoding by the decoder; an instruction register for storing a scan chain controller instruction to be decoded by the decoder; and a scan chain register for storing a scan chain specifying value to be referenced by the scan chain selector to determine which test scan chain to select, wherein the decoder is responsive to the first scan chain controller instruction to simulate as the output of the instruction register the second scan chain controller instruction and to simulate as the output of the scan chain register the predetermined scan chain specifying value, without the contents of the instruction register and scan chain register being updated.

7. An integrated circuit as claimed in claim 6, further comprising a second multiplexer located between the scan chain register and the scan chain selector having a first input connected to the scan chain register and a second input arranged to receive the predetermined scan chain specifying value, the pre-decoder being responsive to the first scan chain controller instruction to cause the second multiplexer to output the data received at the second input.

8. An integrated circuit as claimed in claim 5, further comprising a second multiplexer located between the scan chain register and the scan chain selector having a first input connected to the scan chain register and a second input arranged to receive the predetermined scan chain specifying value, the decoder incorporating a pre-decoder responsive to the first scan chain controller instruction to cause the second multiplexer to output the data received at the second input.

9. An integrated circuit comprising: a plurality of circuit elements; a plurality of serial test scan chains each coupled to a different one of said circuit elements; a scan chain selector responsive to a specified scan chain specifying value to select a corresponding one of said plurality of test scan chains; a scan chain controller having a serial interface for receiving signals from outside of said integrated circuit, said scan chain controller comprising an instruction decoder for decoding scan chain controller instructions received from said serial interface; the decoder being responsive to a first scan chain controller instruction to specify a predetermined scan chain specifying value and a second scan chain controller instruction for decoding by the decoder, wherein one of said circuit elements is an instruction transfer register for specifying an instruction to be executed by a microprocessor of the integrated circuit, and the predetermined scan chain specifying valite identifies a test scan chain incorporating a shift register for shifting data into said instruction transfer register, wherein the decoder is responsive to the second scan chain controller instruction to cause the scan chain selector to be coupled to the serial interface to enable instruction data received at the serial interface to be passed to the shift register of the test scan chain identified by the predetermined scan chain specifying value.

12. An integrated circuit as claimed in claim 11, wherein once data has been written to the data transfer register, the decoder is responsive to a third scan chain controller instruction to cause the scan chain selector to be coupled to the serial interface to enable the data in the data transfer register to be stored into the shift register of the test scan chain coupled to the data transfer register and then output over the serial interface.

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L13: Entry 1 of 1 File: USPT Mar 25, 2003

DOCUMENT-IDENTIFIER: US 6539510 B1
TITLE: Interface board for receiving modular interface cards

Abstract Text (1):
An interface board and inserted modular IC interface cards allows variable length boundary scan chains. The chain can be constructed of any type of programmable integrated circuit (IC) in any order. The interface board contains a plurality of JTAG interfaces that respectively mate with standard adapter interfaces located on the modular IC interface cards. If less than the maximum number of modular IC interface cards are inserted into the interface board, a terminator card is inserted into the standard interface following the last modular IC interface card of the chain. The last test data output signal of the chain is routed back to a connector of the interface board. The interface board includes an output cascade connector that couples with an input cascade connector of another interface board so that any number of interface boards can be cascaded in series to expand the boundary scan chain.

Brief Summary Text (3):
The present invention relates to the field of boundary scan interfaces in accordance with the IEEE 1149.1 standard developed by the Joint Test Action Group (JTAG), and more specifically to the equipment used in connection with circuits employing these boundary scans (hereinafter JTAG) interfaces.

Brief Summary Text (6):
In the past, the JTAG interface was used primarily for testing devices that were soldered or otherwise fixed to a circuit board. Using the JTAG interface, instructions were sent from a computer system to the mounted devices to test for open circuits and short circuits associated with the pins of those devices. Recently, the JTAG interface has been used to program PLDs that are board mounted (i.e. in-system programmable (ISP) devices). To facilitate this programming, multiple PLDs are coupled in a chain in accordance with the IEEE 1149.1 boundary scan standard. The first device in the JTAG chain, which is coupled to the programming computer via a JTAG interface cable, can be programmed and then put into a bypass mode so that other downstream devices in the JTAG chain are programmed sequentially.

Brief Summary Text (11):
In accordance with the present invention, an interface board includes a plurality of JTAG interfaces for receiving one or more modular integrated circuit (IC) interface cards. Each card has a socket of a particular package type for receiving an IC of the same package type and a connector interface, coupled to the socket, for a removable coupling with one of the standard interfaces of the interface board.

Brief Summary Text (12):
The traces of the interface board provide certain JTAG signals, e.g. a test mode select (TMS) signal and a test clock (TCK) signal, to all of the JTAG interfaces (and thus to the modular IC interface cards and ICs in the JTAG chain) in parallel.

Other JTAG signals, e.g. a test data input (TDI) signal and a test data output (TDO) signal, are routed through the ICs in series. Specifically, the TDO signal of one IC becomes the TDI signal of the next IC in the chain. The TDO signal of the last IC in the JTAG chain is provided as a test data final (TDF) signal from the interface board back to a cable (which communicates with the programming system). If less than the maximum number of modular IC interface cards are inserted into the interface board, a terminator card is inserted into the JTAG interface following the last modular IC interface card of the JTAG chain. This terminator card provides the TDF signal.

Drawing Description Text (3):
FIG. 2 illustrates a detailed top view of the interface board of the present invention including the multiple JTAG interface stations.

Detailed Description Text (2):
FIG. 1 illustrates a top view of an interface board 100 of the present invention which includes a plurality of JTAG interface stations 101-106, each station having one of JTAG interfaces 51-56. Note that providing six interface stations 101-106 is exemplary only and that other embodiments of interface board 100 have more or fewer interface stations. Each JTAG interface is designed to receive a modular IC interface card (explained in detail in reference to FIGS. 4, 5A, 5B, and 6) which includes a PLD (or any other JTAG-compliant packaged IC chip). In this embodiment, interface board 100 is wired to create a physical JTAG chain that starts at station 101 and ends at station 106. However, because any modular IC interface card can be connected to any JTAG interface, interface board 100 can support any ordering of devices within the JTAG chain.

Detailed Description Text (3):
A JTAG interface cable 10 is coupled to interface board 100 of the present invention via a cable connector 61 or 65 (both mounted on interface board 100). The other end of cable 10 is adapted to couple to a communication port (e.g., a serial or parallel port) of a standard computer system (not shown). Cable connector 61 is used when cable 10 is coupled to the parallel port of the computer system. On the other hand, cable connector 65 is used when cable 10 is coupled to the serial port of the computer system.

Detailed Description Text (8):
FIG. 2 illustrates another view of interface board 100 of the present invention including its multiple JTAG interface stations 101-106. Each interface station includes: (1) one of JTAG interfaces 51-56; (2) area for a modular IC interface card; (3) one of blocks 41-46 for supporting the modular IC interface card; and (4) connecting traces (shown and described in reference to FIGS. 3A-3D) used to couple JTAG interfaces 51-56 to form the physical JTAG chain.

Detailed Description Text (10):
FIGS. 3A, 3B, 3C, and 3D illustrate a schematic diagram of JTAG interfaces 51-56, cascade connectors 63 and 67, and cable connectors 61 and 65. Cable connector 61 (or cable connector 65) provides JTAG signals from the computer system (not shown) to interface board 100. For example, the TDI (test data input) signal is provided on line 61b; the TCK (test clock) signal is provided on line 61c; and the TMS (test mode select) signal is provided on line 61d. These lines, except line 61b, are coupled to all JTAG interfaces 51-56. Thus, the TCK and TMS signals are provided in parallel to JTAG interfaces 51-56. Line 61b, which provides the TDI signal, is coupled only to JTAG interface 51. The TDO (test data output) signal of JTAG interface 51 is provided as the TDI signal of JTAG interface 52 via line 210. A similar coupling is provided for JTAG interfaces 52-56. Thus, JTAG interfaces 51-56 are coupled in series using lines 210, 218, 212, 214, and 216.

Detailed Description Text (11):
In accordance with one embodiment of the present invention, interface board 100

receives power from either power supply port 73 or an external power connector 75. In one embodiment, power supply 20 (FIG. 1) provides 9V and ground to power supply port 73. A switch 35 provides the 9V supply to voltage regulators 31 and 33 which in turn provide 3.3V and 5V, respectively, to each of JTAG interfaces 51-56 in parallel. Voltage regulators 31 and 33 are coupled to ground (line 79a) via capacitors to stabilize their output voltage. The assignee of the present invention provides a power supply, commercially called the HW-130 universal power supply, but other power supplies of varying voltages, and provided by different manufacturers, can be used within the scope of the present invention.

Detailed Description Text (12):
Alternatively, external power connector 75 provides 3.3 volts and 5 volts to each of JTAG interfaces 51-56 in parallel. Typically, external power connector 75 is used if power supply 20 has another type of connector, i.e. a connector incompatible with power supply port 73, a greater current than that provided by power supply 20 is needed, or voltages other than 3.3 or 5V is required. Note that external power connector 75 can also provide ground to all the JTAG interfaces on line 61a.

Detailed Description Text (16):
FIG. 4 is a schematic diagram of a generic modular IC interface card 300 of the present invention including a socket 305 which can receive any number of different chip packages. Each chip package receives a PLD. Thus, a PLD is inserted into the JTAG chain when its associated modular IC interface card 300 is connected onto a JTAG interface using pins 310a-310e (also referred to herein as standard interface 310). Pin 310a receives the TCK signal, pin 310b receives the TMS signal, pin 310d receives the TDI signal, and pin 310e provides the TDO signal. Pin 310c is reserved for supplying the last TDO output signal in the JTAG chain (i.e. the Test Data Final (TDF) signal) to cable connector 61/65 and therefore is not coupled to socket 305 (as explained in greater detail in reference to FIGS. 3D and 7, the TDF signal is provided by a terminator card or the last JTAG interface in a fully occupied interface board). Pins 310f, 310h, and 310g receive the 3.3V, 5V, and ground voltage, respectively.

Detailed Description Text (18):
FIG. 5A illustrates a top view of one embodiment of a modular IC interface card 300a for one type of chip package. In card 300a, socket 305a is a ball grid array type socket (BGA) which receives a PLD of the same BGA package type. In one embodiment, a standard interface 310 uses top-mounted probe pins including: TDI, GND, TMS, TCK, TDF, and TDO. In this embodiment, a female 18 pin connector 310 (FIG. 5B) located directly underneath the above-mentioned probe pins, is adapted to couple to any one of JTAG interfaces 51-56 of interface board 100 (FIG. 2).

Detailed Description Text (20):
Note that in accordance with the present invention package types of different pin counts and different package types may be used. Thus, a socket 305 may be adapted to receive a very thin plastic quad flat pack (VQ), a plastic quad flat pack (PQ), a thin plastic quad flat pack (TQ), a heat sink plastic quad flat pack (HQ), or a ball grid array (BGA). Exemplary pin counts number from 44 to 208. It is appreciated that any modular IC interface card can be inserted into any of JTAG interfaces 51-56 of JTAG interface board 100 of the present invention.

Detailed Description Text (22):
In accordance with the present invention, the TDO signal from one PLD is provided as the TDI signal of the next PLD in the JTAG chain. The TDO signal of the last PLD in the JTAG chain is routed back as the test data final (TDF) signal to cable connectors 61 and 65 (and thereafter to the computer system for analysis). To provide this signal routing capability in instances where less than all interface stations are occupied, a terminator card 360, illustrated schematically in FIG. 7, is inserted into the JTAG interface station following the last PLD in the JTAG

chain. For example, if a JTAG chain is implemented with interface board 100 having modular IC interface cards plugged into interface stations 101-104, then terminator card 360 is plugged into interface station 105.

Detailed Description Text (23):
In the embodiment shown in FIG. 7, terminator card 360 includes a standard interface 370 (including pins 370a-370h), as well as jumpers 340 and 330 (see modular IC interface card 300 of FIG. 4). Because terminator card 360 provides only routing functionality, pin 370d (receiving the TDO signal) and pin 370c (providing the TDF signal) are the only required pins on terminator card 360. Note that terminator card 360 contains a connector (not shown) located on the bottom side (see, for example, FIG. 5B) for mating with one of JTAG interfaces 51-56 of interface board 100.

Detailed Description Text (24):
Using the above-described configuration, only one terminator card 360 is required for a JTAG chain in accordance with the present invention. On the other hand, if all six interface stations 101-106 of interface board 100 contain PLDs, then terminator card 360 is not required because the TDO pin of JTAG interface 56 (FIG. 3B) can instead be coupled to TDF line 61e via line 220 and jumper 85 (FIG. 3D).

Detailed Description Text (27):
FIG. 9A illustrates a first exemplary configuration 400 of interface board 100 of the present invention in which one modular IC interface card 300a (FIG. 5A) is inserted into JTAG interface 51 (of interface station 101), one terminator card 360a (FIG. 8) is inserted into JTAG interface 52 (of interface station 102), and interface stations 103-106 are unused. In configuration 400, only one PLD, inserted into socket 305a, is within the physical JTAG chain implemented on interface board 100. During programming in configuration 400, JTAG signals (the TDI, TCK, and TMS signals) are applied to cable connector 61 (see FIG. 1) from the computer system (not shown) using cable 10. Terminator card 360a routes the TDO signal from JTAG interface 51 (because JTAG interface 51 is the last in the chain, this TDO signal becomes the TDF signal) back to cable connector 61 via line 61e (FIG. 3A). Cable connector 61 directs the TDF signal back to the computer system using cable 10.

Detailed Description Text (28):
FIG. 9B illustrates a second exemplary configuration 410 of interface board 100. In configuration 410, a first modular IC interface card 300a (FIG. 5A) is inserted into JTAG interface 51, a second modular IC interface card 300c (including a plastic leaded chip carrier socket 305c of the PC44 type) is inserted into JTAG interface 52, modular terminator card 360a (FIG. 8) is inserted into JTAG interface 53, and interface stations 104-106 are unused. In operation, a first PLD is inserted into socket 305a and a second PLD is inserted into socket 305c, thereby providing two programmable IC devices within the JTAG chain. Terminator card 360a routes the TDO signal from JTAG interface 52 (i.e. the TDF signal) back to cable connector 61/65 via line 61e.

Detailed Description Text (29):
FIG. 9C illustrates a third exemplary configuration 420 of interface board 100 in which six modular IC interface cards 300a, 300c, 300d, 300b', 300b, and 300e are respectively inserted into JTAG interfaces 51-56. First and second modular IC interface cards 305a and 300c are the same as described in reference to FIG. 9B. A third modular IC interface card 300d uses a plastic quad flat pack socket 305d of the PQ100 type; a fourth modular IC interface card 300b' uses a plastic leaded chip carrier socket 305b' of the PC84 type; a fifth modular IC interface card 300b uses a plastic leaded chip carrier socket 305b' of the PC84 type; and a sixth modular IC interface card 300e uses a very thin quad flat pack of the VQ44 type. In operation, PLDs are inserted into sockets 305a, 305b', 305b, 305c, 305d, and 305e, thereby providing six programmable IC devices within the JTAG chain. Because no other interface board is cascaded to interface board 100, jumper 85 is placed to couple

lines 220 and 61e (FIG. 3D), thereby transferring the TDO signal (now TDF signal) from JTAG interface 56 back to cable connector 61/65.

Detailed Description Text (33):
Note that jumper 85 (FIG. 3D) is switched to a position labeled CABLE if JTAG interface station 106 is occupied with a modular IC interface card and either is the only interface board used in a JTAG chain or is the last downstream interface board in a series of interface boards. In this configuration, line 220 (providing the TDO signal) of interface station 106 is coupled to line 61e (providing the TDF signal to cable connector 61/65). Jumper 85 is switched to a position labeled TDO if JTAG interface station 106 is occupied with a modular IC interface card and is not the only interface board used in a JTAG chain nor is the last downstream interface board in a series of interface boards. In this configuration, line 220 (providing the TDO signal) of interface station 106 is coupled to line 69 (which transfers this TDO signal as the TDI signal to line 61b of input cascade connector 67). In all other instances, jumper 85 may be switched to either position, i.e. a "don't care" configuration.

CLAIMS:

1. A system for implementing a boundary scan chain, said system comprising: an interface board comprising: a connector for transferring boundary scan signals; and a plurality of interfaces coupled in series in a predetermined order, and in parallel to receive a plurality of said boundary scan signals; and at least one card comprising: a socket for receiving an integrated circuit; and a connector interface, coupled to said socket, for removably coupling with one of said plurality of interfaces.